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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/729,111	12/05/2003	Daryl D. Starr	ALA-026	3130

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EXAMINER	
WILSON, ROBERT W	

ART UNIT	PAPER NUMBER
2661	

DATE MAILED: 06/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/729,111	STARR ET AL.	
	Examiner	Art Unit	
	Robert W. Wilson	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,6-9,11,14 and 19-23* is/are rejected.

7)☒ Claim(s) *2,5,10,12,13 and 15-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

PHIRIN SAM
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/8/04, [redacted], 1/26/04, 6/10/04, d*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

1.0 The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2.0 Claims 1,3-4,6-9, 11, 14, 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jolitz (Patent Pub: 2001/0025315) in view of Connery (U.S. Patent No.; 5,937,169)

Referring to claim 1, Jolitz teaches: A Network Accelerator (TCP offload engine) per Fig 1 which is connected to a host per Pg 3 Para [0032] and which has registers and ADE 2 (First memory) in which expected values associated with TCP/IP headers are stored per Pg 7 Para [0076]. The RX engine in the Network Accelerator stores TCP/IP header values in the Proto memory and RX register (second memory) per Pg 7 Para [0077]. The applicant broadly defines a "flush detect signal indicative of whether an error has occurred". The RX engine (140 per Fig 6) has a header matcher with logic (150 per Fig 6 or Pg 7 Para [0077] which determines if there is a match otherwise the packet is routed to Rx bypass memory or flushed. The reference further teaches in the event that an error is recognized then the operation is suspended which the examiner interprets as a "flush detect signal indicative of whether an error has occurred".

Jolitz does not expressly call for: two specific values of packet header: such as, packet sequence number or packet acknowledgment number but teaches that static values of TCP/IP headers are utilized for comparison.

Connery teaches: that sequence number and acknowledgment number as well as window are standard static values in a TCP/IP header per Fig 4.

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the sequence number and acknowledgment number of Connery in the accelerator of Jolitz because they are standard static values in a TCP/IP header.

In Addition the combination teaches:

Regarding claim 4, The combination of Jolitz and Connery teaches the TOE of claim 1 wherein two values are utilized simultaneously

Jolitz teaches: Window or third value in the packet header per Fig 4.

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the sequence number and acknowledgment number of Connery in the accelerator of Jolitz because they are standard static values in a TCP/IP header.

In Addition Jolitz teaches:

Regarding claim 3, Jolitz teaches checking relative to header values and there are at least two header values.

Regarding claim 6, Jolitz teaches: output is performed at the same rate as the signal clock per Pg 3 Para [0029] or approximately one clock period.

Regarding claim 7, Jolitz teaches: The RX engine (140 per Fig 6) has a header matcher with logic (150 per Fig 6 or Pg 7 Para [0077] which determines if there is a match or state machine that does not fetch instructions, decode instructions, and execute the instructions.

Regarding claim 8, Jolitz teaches: output is performed at the same rate as the signal clock per Pg 3 Para [0029] or approximately one clock period.

Regarding claim 9, Jolitz teaches: that memory 24 per Pgs 5 Para [0045] has a shadowed copy or stack that is passed onto the host system.

Referring to claim 11, Jolitz teaches: A Network Accelerator (TCP offload engine) per Fig 1 which has registers and ADE 2 (First memory) in which expected values associated with TCP/IP headers are stored per Pg 7 Para [0076]. The RX engine in the Network Accelerator stores TCP/IP header values in the Proto memory and RX register (second memory) per Pg 7 Para [0077]. The applicant broadly defines a "signal indicative of whether an exception condition has occurred". The RX engine (140 per Fig 6) (hardware state machine) has a header matcher with logic (150 per Fig 6 or Pg 7 Para [0077] which determines if there is a match otherwise the packet is routed to Rx bypass memory or in the event that an error is recognized then the operation is suspended which the examiner interprets as a "signal indicative of whether an exception condition has occurred". Jolitz teaches that the output of the accelerator runs at eth same clock rate as the signaling per Pg 3 Para [0029] or wherein the hardware state machine is clocked by a clock signalaand output a decision within approximately one period of the clock signal.

Jolitz does not expressly call for: two specific values of packet header: such as, packet sequence number or packet acknowledgment number but teaches that static values of TCP/IP headers are utilized for comparison.

Connery teaches: that sequence number and acknowledgment number as well as window are standard static values in a TCP/IP header per Fig 4.

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the sequence number and acknowledgment number of Connery in the accelerator of Jolitz because they are standard static values in a TCP/IP header.

In Addition Jolitz teaches:

Regarding claim 14, Jolitz teaches: The RX engine (140 per Fig 6) has a header matcher with logic (150 per Fig 6 or Pg 7 Para [0077] which determines if there is a match otherwise the packet is routed to Rx bypass memory and processing is turned over to the host."

Referring to claim 19, Jolitz teaches: A Network Accelerator (TCP offload engine) per Fig 1 which has registers and ADE 2 (First memory) in which expected values associated with TCP/IP headers are stored per Pg 7 Para [0076].
The RX engine in the Network Accelerator stores TCP/IP header values in the Proto memory and RX register (means for receiving) per Pg 7 Para [0077]. The applicant broadly defines a "exception has occurred". The RX engine (140 per Fig 6) has a header matcher with logic (150 per Fig 6) or Pg 7 Para [0077] which determines if there is a match otherwise the packet is routed to Rx bypass memory or in the event that an error is recognized then the operation is suspended which the examiner interprets as a "signal indicative of whether an exception condition has occurred". Jolitz teaches that the output of the accelerator runs at the same clock rate as the signaling per Pg 3 Para [0029] or wherein the hardware state machine is clocked by a clock signal and output a decision within approximately one period of the clock signal.

Jolitz does not expressly call for: two specific values of packet header: such as, packet sequence number or packet acknowledgment number but teaches that static values of TCP/IP headers are utilized for comparison.

Connery teaches: that sequence number and acknowledgment number as well as window are standard static values in a TCP/IP header per Fig 4.

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the sequence number and acknowledgment number of Connery in the accelerator of Jolitz because they are standard static values in a TCP/IP header.

In Addition Jolitz teaches:

Regarding claim 20, Jolitz teaches Proto memory and Rx Reg which is means for storing at least two values.

Regarding claim 21, Jolitz teaches: Expected TCP header values are written into registers and ADE 2 (memory) in which expected values associated with TCP/IP headers are stored per Pg 7 Para [0076].

Regarding claim 22, Jolitz teaches: The RX engine (140 per Fig 6) has a header matcher with logic (150 per Fig 6 or Pg 7 Para [0077] which determines if there is a match otherwise the packet is routed to Rx bypass memory or no sequential logic elements in which the means consists entirely of combinatorial logic elements.

Regarding claim 23, Jolitz teaches expected values of the TCP/IP header are compared to the actual values of the TCP/IP header which the examiner interprets as a state machine.

Regarding claim 24, Jolitz teaches that if there is not a match then processing is passed to the host per Pg 5 Para [0051]

Claim Objections

4.0 Claims 2, 5, 10, 13, & 15-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5.0 The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. Elzur (Patent Pub No.: US2004/0042646) which teaches a TCP Offload Engine (TOE) per Fig 1 which keeps track of sequence numbers and windows per Pg 4 Paragraphs [0032]-0036]. A stack is utilized between the TOE and the host per Pg 2 Para [0019] . The TOE utilizes a state machine per Pg 5 Para [0046].
2. Rajagoplan (Patent Pub No.: US2004/0249998 A1) which teaches a Hot Unit which has a transmit and receive engine. The transmit engine stores acknowledgment state, windows, and sequence numbers in a DCT table per Pg 3 Paragraphs [0046]-[0047]. A Parsing unit determines if the sequence number in the DCT table equals the received sequence number per Pg 9 Paragraphs [0098]-[0101] and Figure 8B.
3. Vangal (Patent Pub No.; 2004/0193733 A1) teaches a Network Protocol Offload Engine that compares the newly received packet sequence numbers to the expected sequence number per Pg 6 Para [0066]. The output clock cycle matches the input clock cycle per Fig 16.
4. Vangal (Patent Pub No.: 2004/0125751 A1) teaches a Transport Control Offload Engine (TOE) . the engine parses the received packet header in to buffers per Pg 3 Para [0045]. The TOE determines if the incoming ACK and sequence Numbers are valid per Pg 6 Para [0073].
5. Minami (Patent Pub No.: US2004/0062267) which teaches that receive/transmit limit valid values are bits which indicate if a sequence number is wrapped around and is associated with security per Pg 59.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert W. Wilson whose telephone number is 571/272-3075. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau T. Nguyen can be reached on 571/272-3126. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Robert W. Wilson
Robert W Wilson
Examiner
Art Unit 2661

RWW
5/12/05

PHIRIN SAM
PRIMARY EXAMINER